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Interconnectivity

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ISP1122 USB Hub Demonstration Board

User's Manual

Revision 1.01

ISP1122 USB Hub Demonstration Board - User's Manual

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PREFACE

The Philips Semiconductors Hub ISP1122 is a state of the art, 3rd generation, stand-alone USB hub controller IC that complies with the latest USB Spec Rev 1.1. The major priorities for us during the design were:

1. Interoperability
2. Reduction in the overall system cost
3. System designer friendly product

We have relied on more than 3 years of our USB design and customer support experience to achieve these objectives. Today our USB products already provide an industry benchmark for the interoperability tests. Since interoperability problems result in the most expensive failures in the field, we have further tightened the design specifications to address many ambiguities. The IC has integrated many functions and offers features that reduce the major components of the total system cost. We have employed many design techniques to reduce the EMI emissions, increase the ESD resiliency and improve the manufacturing test criteria to insure a high quality product. We estimate that the ISP1122 enables cost reductions exceeding the cost of the IC itself!!!

Our overall ambition is to provide you with the Peace of Mind for using our products in the total system solution. We welcome your comments and suggestions to help us improve. For more information about the ISP1122 and the latest updates to the design support documents, please visit the web site http://www.flexiusb.com/.

With Best Regards,

Team Members of the Asia Product Innovation Center

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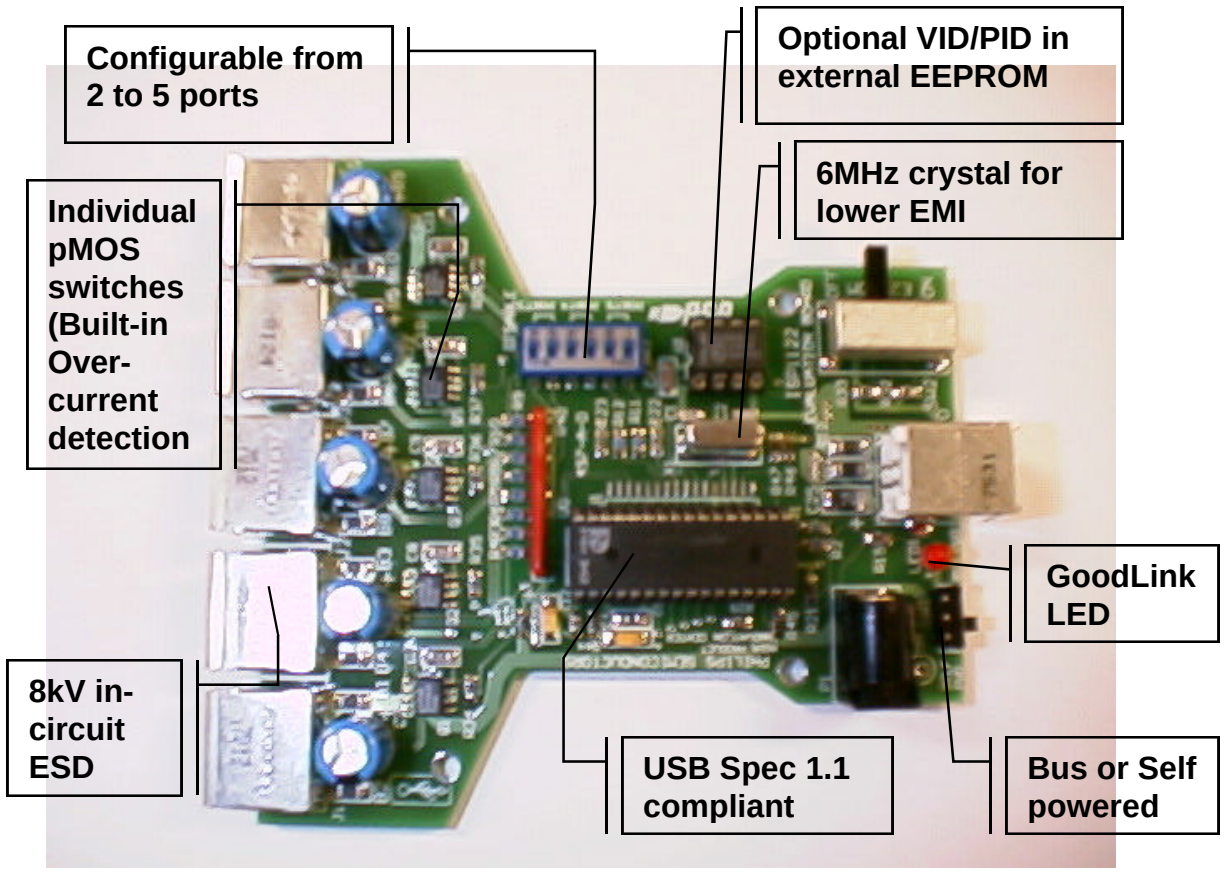
1. INTRODUCTION

The ISP1122 demonstration board (simply called demo board in the following text) is designed for evaluating the features and functionality of the ISP1122 IC. This manual explains the schematic of the ISP1122 demo board, demonstrates the PCB layout, shows the complete BOM (Bill of Material) and describes the detailed usage of every switch on the board.

1.1. Demo board Features

- USB Spec Rev 1.1 compliant
- Selectable bus or self/hybrid-powered operation
- Configurable number of downstream ports from 2 to 5
- Customizable Vendor ID and Product ID through EEPROM
- Individual power switching and individual overcurrent protection
- Hub health indicator through GoodLink™ LED
- Verified interoperability with many systems and peripherals (Check the continuously updated Interoperability report on the web site)
- FCC Part 15 , Subpart J, Class B compliant (pending)
- UL approved (pending)
- 8 kV ESD



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2. BOARD DESCRIPTION

2.1. Configuration modes

The INDV, OPTION and SP/BP_N pins determine hub configuration modes. Users can either set these signals to logic high or low. The INDV and OPTION pins can also be used for connections to external E2PROM. This allows for customized Vendor ID and Product ID among other configuration modes. The E2PROM contents will be discussed in later text.

The meanings of the three configuration pins are described in Table 1.

Table 1. Mode configuration pins

Name	Value	Description	Other Usage
INDV	0	Gang power switching and global over-current protection mode.	SCL
	1*	Individual power switching and individual over-current protection mode.	
OPTION	0	Both power switch and over-current protection functions are active.	SDA
	1*	Either one of Power switch control or over-current protection functions are active depending on self-powered or bus-powered configuration. For self-powered operation, the power switch control is optional and for bus-powered operation, the over-current protection is optional.	
SP/BP_N	0	Bus-powered mode.	
	1	Self-powered or hybrid powered mode.	Local Power Lost Indication

1* signifies a pull-up high.

Note: The ISP1122 also supports hybrid self-powered mode. In this mode, the hub controller draws power from upstream Vbus and local power is used for downstream ports. Hybrid powered mode is advantageous to differentiate between a disconnected and an unpowered device. This makes it possible to keep communicating between the host and the device/hub even if local power is lost.

Each composite setting of the three pins determines one configuration mode of the hub. So the ISP1122 can be configured into eight different modes. Table 2 shows these configuration modes.

Table 2a. Mode selection table

Mode	INDV	OPTION	SP/BP_N	PSW1,2,3,4_N	PSW5_N	OC1,2,3,4_N	OC5_N
0	0	0	0	GL1,2,3,4_N	GPSW_N	Inactive	GOC_N
1	0	0	1	GL1,2,3,4_N	GPSW_N	Inactive	GOC_N
2	0	1	0	GL1,2,3,4_N	GPSW_N	Inactive	Inactive
3	0	1	1	GL1,2,3,4_N	GL5_N	Inactive	GOC_N
4	1	0	0	PSW1,2,3,4_N	Inactive	OC1,2,3,4_N	Inactive
5	1	0	1	PSW1,2,3,4_N	PSW5_N	OC1,2,3,4_N	OC5_N
6	1	1	0	PSW1,2,3,4_N	Inactive	Inactive	Inactive
7	1	1	1	GL1,2,3,4_N	GL5_N	OC1,2,3,4_N	OC5_N

Inactive OCX_N pins need to be tied to Vcc.

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Table 2b. Mode selection table ('ctd)

Mode	Self-/Bus-Powered	Power Switch control	GoodLink	Over-current Protection	Remarks
0	Bus-powered	Ganged	Yes*	Global	Ganged and bus powered
1	Self-powered	Ganged	Yes*	Global	Ganged and self powered
2	Bus-powered	Ganged	Yes*	Inactive	No overcurrent
3	Self-powered	Inactive	Yes	Global	No power switch control
4	Bus-powered	Individual*	No	Individual*	Individual and bus powered
5	Self-powered	Individual	No	Individual	Individual and self powered
6	Bus-powered	Individual*	No	Inactive	No overcurrent
7	Self-powered	Inactive	Yes	Individual	No Power switch control

* Without Port 5

The demo board implements modes 4 and 5 as selected by switch SW1 (see Table 3). In these two modes, the hub supports individual power control and individual over-current protection for downstream ports.

Table 3. Bus/Self-powered selection switch

SW1	Selection
1-3	Bus powered
1-2	Self/Hybrid powered

WARNING:
When supplying power through the DC jack, make sure that SW1 is at position 1-2 indicating a self-powered mode. If SW1 is at position 1-3 (bus-powered mode), the upstream supply and the local supply will be shorted!

2.2. EEPROM support

INDV and OPTION pins can also be connected to external serial EEPROM for Vendor ID, Product ID customization and configuration setting. The interfacing protocol is I2C. The ISP1122 acts as the master and the EEPROM as the slave. The I2C clock frequency generated by the ISP1122 is slightly less than 100 k bit/s to support low end EEPROM. The following EEPROM models have been proven suitable: PCA8581, PCF8582C-2, 24C00, 24C01. Both the SCL (OPTION) and SDA (INDV) pins need to be pulled up to Vcc; a 3.3k ohm value is recommended.

On power on, the ISP1122 detects the presence of the EEPROM through the Signature byte (=AAh). If the signature is correct, the content of the E2PROM will overwrite the default setting. The content of the EEPROM is listed in Table 4 and the meaning of the configuration bits are listed in Table 5.

Table 4. EEPROM Content

Address	Content							
0	*idVendor* lower byte (default = CCh)							
1	*idVendor* higher byte (default = 04h)							
2	*idProduct* lower byte (default = 22h)							
3	*idProduct* higher byte (default = 11h)							
4	C7	C6	C5	C4	C3	C2	C1	C0
5	Signature = AAh							

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Table 5. Configuration Bit

Bit	Name	Value	Meaning
C0	OPTION		Refer to mode selection table.
C1	INDV		Refer to mode selection table.
C2	RESERVED	0*	Should always be programmed to '0'.
C3	PwrOn2PwrGood	0* 1	Modifies the Hub Descriptor Field *PwrOn2PwrGood*. 100 ms (32h) 500 ms (FAh)
C4	String Descriptor Enable	0* 1	Disable String Descriptor Enable String Descriptor (String is "Philips Semiconductors" and "ISP1122").
C5	Internal Analog Overcurrent Detection Enable	0 1*	Disable internal analog overcurrent detection circuit. When disabled, the overcurrent pins OCX_N convert to digital (TTL) level. Enable internal analog overcurrent detection Circuit.
C7:6	MaxPower	00* 01 1X	Modifies the Configuration Descriptor Field *MaxPower*. 100 mA (32h) 500 mA (FAh) 0 mA (00h)

Note: * denotes the internal default value when EEPROM is not present.

Although the C0 (OPTION) and C1 (INDV) bits can be programmed to any value, the demo board hardware only supports Modes 4 and 5. That means these two bits must be programmed with

C0 (OPTION) = 0
C1 (INDV) = 1

in order to work in this demo board.

The EEPROM can be disabled through switch SW2 as shown in Table 6. When the EEPROM is not present, switch SW2 has to be set to "EEPROM disabled" state to correctly configure the board in the right mode of operation (Modes 4 or 5).

Table 6. EEPROM enable/disable switch

SW2	EEPROM
1-3	EEPROM enabled
1-2	EEPROM disabled

2.3. Number of Downstream Ports

The ISP1122 number of downstream ports can also be configured from 5 to 2. For bus-powered mode, USB spec only allows for 4 downstream ports. The port number configuration is set through switch SW3 and is listed in Table 7.

Table 7. Number of Downstream Ports Setting (SW3)

1-12 2-11	3-10 4-9	5-8 6-7	Number of Downstream Ports
OFF	OFF	OFF	5
ON	OFF	OFF	4
ON	ON	OFF	3
ON	ON	ON	2
Other combinations			Illegal

Note: Bus-powered mode can only have 4 downstream ports according to USB spec.

2.4. Factory Default Setting

The factory default setting of the configuration switches are shown in Table 8.

Table 8. Factory Default Setting

Switch	Selection	Default
SW1	Self/Bus-powered	Bus-powered
SW2	EEPROM	No EEPROM (disabled)
SW3	Number of Downstream Ports	4

2.5. PCB layout consideration

The following PCB layout considerations are employed:

1. Route signal traces on the top layer as much as possible. The bottom layer is reserved for ground routing. This should minimize EMI issues.
2. Power traces need to be thick to meet USB spec voltage drop requirement.
3. Put 150 uF capacitors as close as possible to the downstream ports. These capacitors, together with ferrite beads minimize voltage droop upon downstream ports hot insertion.
4. Route each pair of the D+ and D- lines close and parallel to each other and their length should be equalized. This will ensure good symmetrical differential signal swing that enhances interoperability and also lower EMI.
5. Crystal oscillator should be placed close to the ISP1122.
6. Decoupling capacitors for the ISP1122 Vcc and V3.3 signals should be placed close to the pins.

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3. Appendix

3.1. ISP1122 Pin Diagram

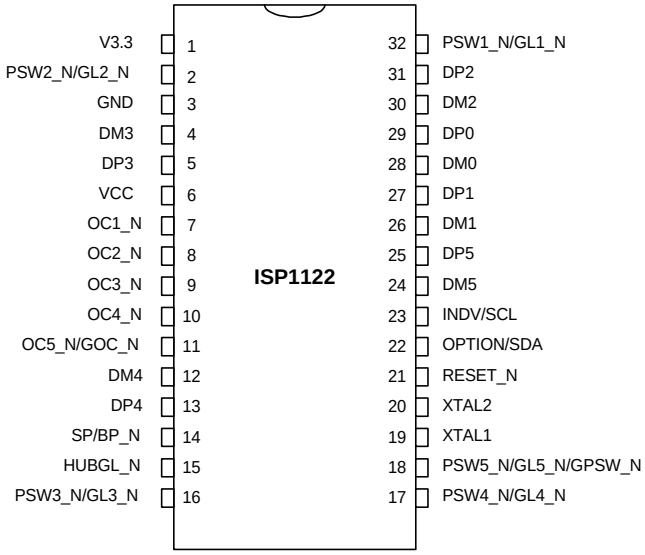

Figure 1. Pin diagram of ISP1122

3.2. Schematic Diagram

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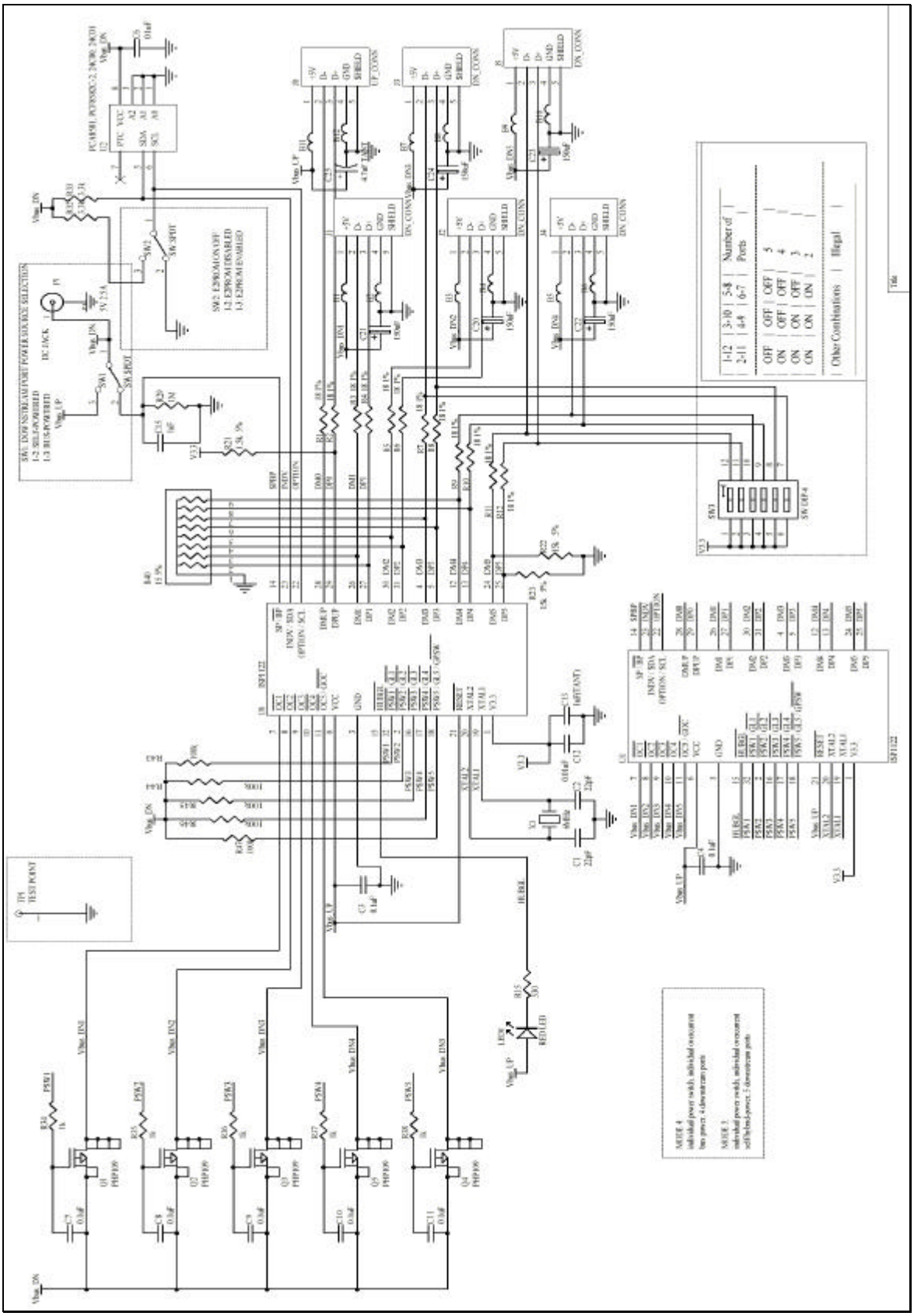

Figure 2. Schematic diagram of the ISP1122 demo board

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3.3. Bill of Material (BOM) List

Part #	Part Type	Designator	Qty
1	0.01uF. High frequency decoupling capacitors	C3, C12	2
1	0.1uF. High frequency decoupling capacitor	C6	1
12	1uF (TANT). Low frequency decoupling capacitors	C4, C13	2
16	4.7uF TANT. Upstream bulk capacitor	C25	1
6	150uF. Downstream bulk capacitors for meeting voltage droop requirement	C20, C21, C22, C23, C24	5
2	0.1uF. Snubber capacitors for power switching	C7, C8, C9, C10, C11	5
9	1k ohm. Snubber resistors for power switching	R34, R35, R36, R37, R38	5
4	100k ohm. Open drain pull-up resistors for power switch control.	R43, R44, R45, R46, R47	5
3	1.5k ohm 5%. Upstream pull-up resistor	R21	1
5	15k ohm 5%. Downstream pull-down resistor package	R40	1
7	15k ohm 5%. Downstream port 5 pull-down resistor	R22, R23	2
8	18 ohm 1%. Impedance matching resistors	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12	12
10	1M ohm. Pull-down resistor for self/bus-powered mode and local power loss detection	R29	1
11	1uF. Capacitor for self/bus-powered mode detection	C15	1
13	22pF. Crystal oscillator capacitors	C1, C2	2
14	3.3k ohm. I2C pull-up resistors	R32, R33	2
15	330 ohm. LED current limiting resistors.	R15	1
17	6MHz. Crystal oscillator	X1	1
18	5V/2.5A DC JACK. DC power supply jack for self-powered mode	P1	1
19	USB "A" Receptacle. Downstream port connectors	J1, J2, J3, J4, J5	5
20	USB "B" Receptacle. Upstream port connector	J0	1
21	Ferrite beads. Beads for EMI and in-rush current limiting	B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12	12
22	ISP1122. Philips Semiconductors USB Hub controller (SDIP32 package)	U0	1
23	ISP1122. Philips Semiconductors USB Hub controller (SO32 package)	U1	1
24	PCA8581C/PCF8582C-2/24C00/24C01. EEPROM with I2C interface	U2	1
25	PHP109. PMOS power transistor	Q1, Q2, Q3, Q4, Q5	5
26	LED	LED1	1
27	Switch DIP-6. Switch for number of downstream ports configuration	SW3	1
28	Switch SPDT. EEPROM enable switch	SW2	1
29	Switch SPDT. Self/Bus-powered selection switch	SW1	1
30	TEST POINT	TP1	1

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3.4. Component Placement

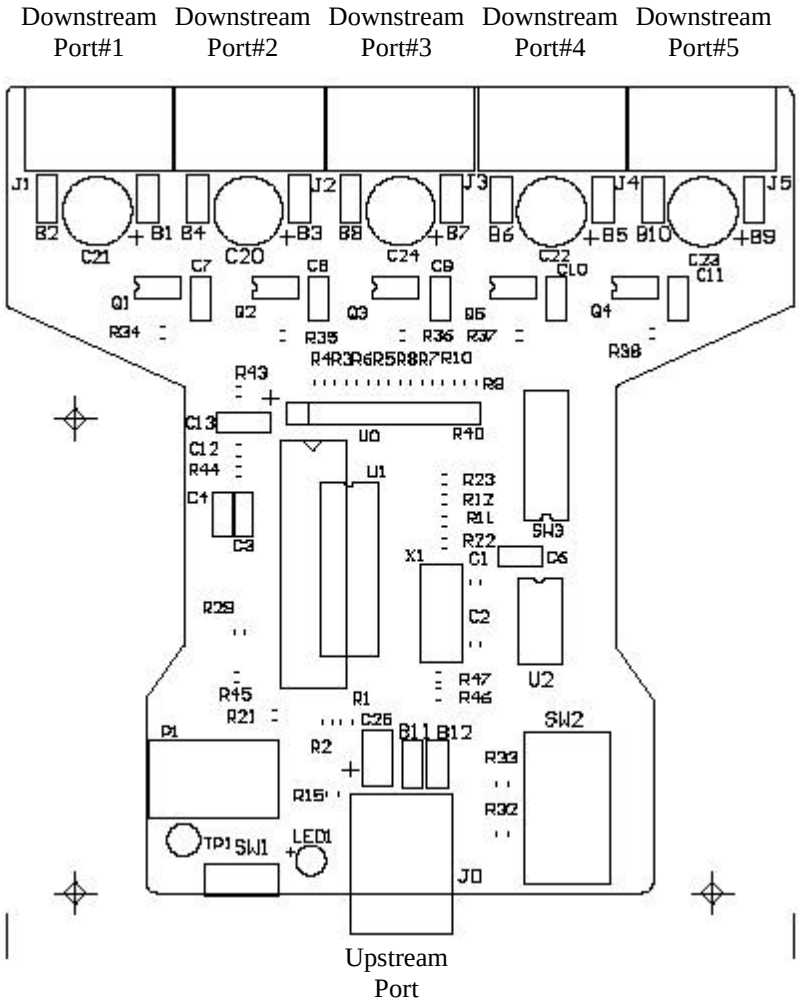

Figure 3. Component placement of ISP1122 demo board

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3.5. PCB Layout

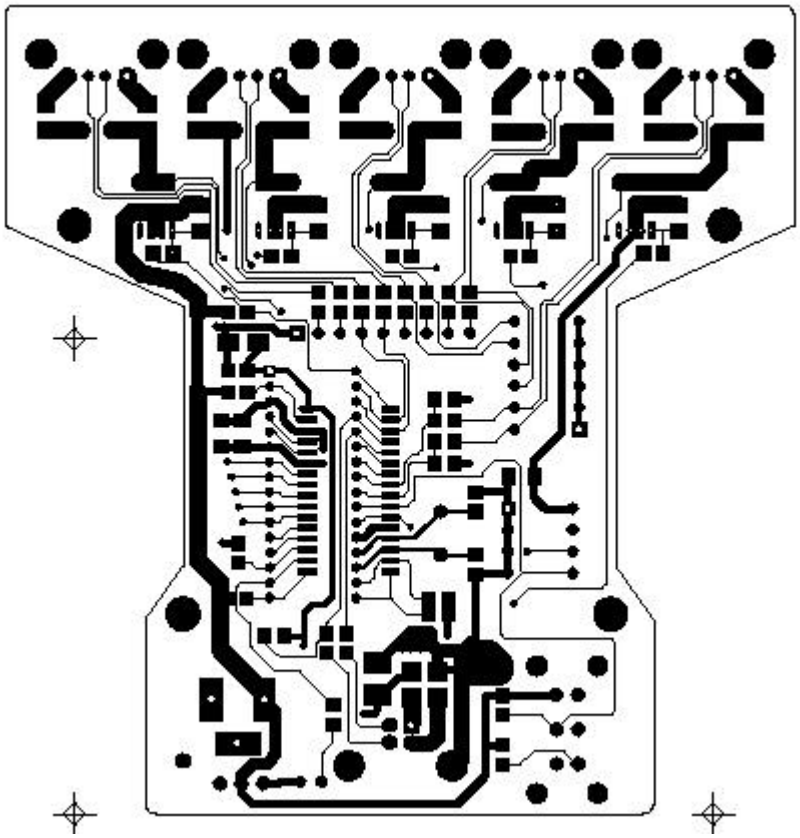

Figure 4. Top Layer PCB Layout

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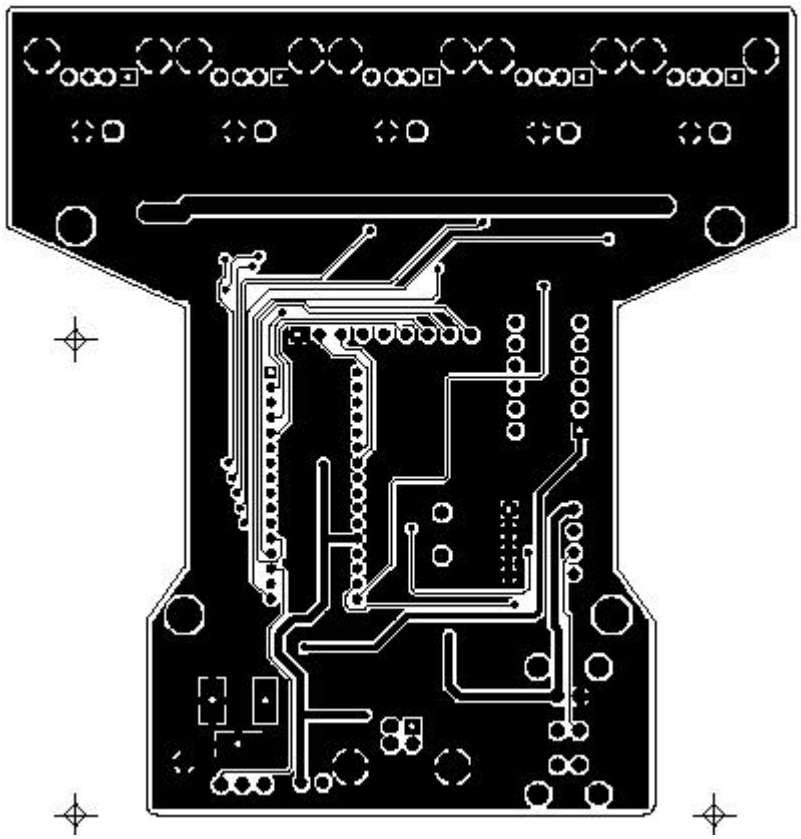

Figure 5. Bottom Layer PCB Layout